REMARKS

The Final Office Action mailed May 16, 2003, has been received and reviewed. Claims 23 through 33 are currently pending in the application. All claims stand rejected. Applicants propose to amend the Title of the Invention and claims 23 through 26, 29 and 31 as hereinabove set forth. Reconsideration of the application in light of the proposed amendments and the following remarks is respectfully requested.

Proposed Title Amendments

Applicants have proposed to amend the Title of the Invention as hereinabove set forth to more accurately reflect that which is claimed in the present application. It is respectfully submitted that no new matter is added by the proposed amendment and that the proposed amendment is supported by the as-filed application and drawings. Please enter the Title of the Invention as proposed to be amended herein.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent 5,472,896 to Chen et al.

Claims 23 through 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,472,896 to Chen et al. (hereinafter the "Chen reference"). As the Chen reference fails to disclose, either expressly or inherently, each and every element as set forth in the rejected claims, Applicants respectfully traverse this rejection.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Chen reference discloses, in a first embodiment, a MOSFET device, and a method for fabricating the same, having a gate oxide layer 12 formed over a semiconductor substrate 10, a polysilicon layer 14 formed over the gate oxide layer 12 and a refractory metal silicide layer 16

formed over the polysilicon layer 14. *See, Chen reference*, col. 1, line 57–col. 2, line 5; col. 4, lines 29–36; FIG. 3b. In fabricating the device of the first embodiment, subsequent to formation of the refractory metal silicide layer 16, the structure is etched down to the gate oxide layer 12 as shown in FIG. 3b. Subsequently, a first thin oxide layer 18 is formed over the exposed surfaces of the gate oxide layer 12, the polysilicon layer 14, the refractory metal silicide layer 16 and the semiconductor substrate 10 by thermal oxidation. This thermal treatment transforms the refractory metal silicide layer 16 from its amorphous form into a crystalline form. *See id.*, col. 2, lines 14 – 20; FIGs. 3c and 4c. Next, a second oxide layer 20 is formed over the first thin oxide layer 18 and the two oxide layers 18, 20 are etched back to form sidewall spacers 20 on the side walls of the gate electrode structure. *See id.*, col. 2, lines 26–34. After formation of the sidewall spacers 20, an ion implantation step is performed to transform the refractory metal silicide layer 16 from its crystalline form back into the amorphous form. *See id.*, col. 4, lines 36–42. Subsequently, a second thin oxide layer 22 is formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10, preferably by conventional thermal oxidation. *See id.*, col. 2, lines 36–39; col. 4, lines 45–49.

In a second embodiment, the MOSFET device of the Chen reference further includes a polysilicon barrier cap layer 30 formed over the refractory metal silicide layer 16, preferably by chemical vapor deposition (CVD). *See id.*, col. 4, line 65–col. 5, line 8; FIG. 4b. Due to the thermal treatment of the CVD process, the refractory metal silicide layer 16 is transformed from the amorphous form into a crystalline form upon deposition of the barrier cap layer 30. *See id.* In fabricating the device of this second embodiment, subsequent to deposition of the barrier cap layer 30 (and thus transformation from the amorphous form into a crystalline form), the barrier cap layer 30, the refractory metal silicide layer 16 and the polysilicon layer 14 are etched down to the gate oxide layer 12 as shown in FIG. 4b. After formation of the gate electrode structure, ion implantation is performed to transform the refractory metal silicide layer 16 back into the amorphous form. *See id.*, col. 5, lines 9–25. The MOSFET device is then completed as described above with regard to the first embodiment.

As recognized by both the Specification of the present application and the Chen reference, high temperature steps during fabrication of gate stack structures (*e.g.*, thermal oxidation, CVD and the like) cause the formation of silicon clusters within the metallic silicide film. *See, Specification*, page 5, lines 19–21; *Chen reference*, col. 2, lines 49–53 and col. 5, lines 5–8. The Specification of the present application indicates pitting is caused on the dielectric layer during gate stack etching by the presence of such silicon clusters inside the metallic silicide film. *See, Specification*, page 5, lines 24–26. Specifically, the etch rate of silicon clusters has been found to be approximately 1.2 times that of the metallic silicide film (in the case of a tungsten silicide film) during gate stack etch. Accordingly, the silicon clusters etch tunnels into the metallic silicide film at each silicon cluster. This tunneling, in turn, is translated into the surface of the gate dielectric layer and, thereby, pits are formed. *See id.*, page 5, line 24–page 6, line 2. If the pits are deep enough to extend through the gate dielectric layer and into the silicon substrate, junction leakage, refresh problems and potential destruction of the component may occur. *See id.*, page 3, line 27–page 4, line 2.

It is respectfully submitted that the Chen reference fails to disclose, either expressly or inherently, a gate stack or semiconductor device comprising a gate stack, on a silicon substrate having a dielectric layer thereover, wherein the dielectric layer is substantially devoid of pitting and wherein the gate stack includes a dielectric cap comprising silicon nitride on a metallic silicide film, as claimed in the present application (as the claims are proposed to be amended herein).

Independent claim 23, as proposed to be amended herein, recites an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. The operable gate stack includes a non-crystalline metallic silicide film and a dielectric cap comprising silicon nitride on the non-crystalline metallic silicide film.

It is respectfully submitted that the Chen reference, in the first embodiment thereof described above, does not disclose a dielectric cap *comprising silicon nitride* on the refractory metal silicide layer 16 thereof. It is stated in the Final Office Action that the second thin oxide layer 22 constitutes a dielectric cap layer over the refractory metal silicide layer 16. *See, Final*

Office Action, page 2, ¶2; page 5, ¶2. However, the layer disclosed by the Chen reference is an oxide layer and not a layer *comprising silicon nitride* as recited in independent claim 23, as proposed to be amended herein. Accordingly, it is respectfully submitted that such embodiment does not anticipate independent claim 23, as proposed to be amended herein. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

With regard to the second embodiment of the Chen reference, it is respectfully submitted that the dielectric layer of the MOSFET device so described is not "substantially devoid of pitting" as recited in independent claim 23, as proposed to be amended herein. As previously described, during formation of the device of the second embodiment described in the Chen reference, the gate electrode structure is etched *subsequent to* deposition of the barrier cap layer 30 and *prior to* ion implantation being performed on the refractory metal silicide layer 16. *See, Chen reference*, col. 4, line 65–col. 5, line 8; FIG. 4b. Upon deposition of the barrier cap layer 30, silicon crystals are formed in the refractory metal silicide layer 16. *See id.* Accordingly, when the gate electrode structure is subsequently etched, silicon crystals are present in the refractory metal silicide layer 16. Only after etching of the gate electrode structure is the refractory metal silicide layer 16 implanted with ions to transform the refractory metal silicide layer 16 back into the amorphous state. *See id.*, col. 5, lines 9–5. Thus, since the gate electrode structure is etched *while the silicon crystals are present in the refractory metal silicide layer 16*, it is respectfully submitted that the dielectric layer contains pits caused by the difference in the etch rate of the silicon crystals relative to the refractory metal silicide layer 16. *See, Specification*, page 5, line 24–page 6, line 2.

Further, it is respectfully submitted that the barrier cap layer 30 disclosed by the Chen reference is not a dielectric cap *comprising silicon nitride* as recited in independent claim 23, as proposed to be amended herein. Rather, the barrier cap layer 30 of the Chen reference is a polysilicon layer. *See, Chen reference*, col. 5, lines 3–5. Thus, independent claim 23, as proposed to be amended herein, is not anticipated by the second embodiment disclosed by the Chen reference.

It is stated in the Final Office Action that Applicants argument that the dielectric layer of the Chen reference is devoid of pitting is not persuasive as the Chen reference contains disclosure wherein the gate oxide layer 12, the polysilicon layer 14 and the refractory metal silicide layer 16 are etched prior to the refractory metal silicide layer 16 being transformed from an amorphous state to a crystalline state. *See*, *Final Office Action*, page 5, ¶3. It is respectfully submitted, however, that this argument applies only to the second embodiment disclosed by the Chen reference and that the disclosure relied upon by the Examiner in making the above statement is disclosure regarding the first embodiment of the Chen reference.

Independent claim 24, as proposed to be amended herein, recites an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. The operable gate stack includes an amorphous metallic silicide film which is substantially devoid of silicon clusters and a dielectric cap comprising silicon nitride on the amorphous metallic silicide film.

As discussed with regard to independent claim 23 above, the first embodiment disclosed by the Chen reference fails to disclose, either expressly or inherently, an operable gate stack having a dielectric cap *comprising silicon nitride* on a non-crystalline metallic silicide film as recited in independent claim 24, as proposed to be amended herein. Rather, the dielectric cap of the first embodiment of the Chen reference is an oxide layer, *i.e.*, thin oxide layer 22. As such, it is respectfully submitted that the first embodiment disclosed by the Chen reference fails to anticipate independent claim 23, as proposed to be amended herein.

Further, it is respectfully submitted that the second embodiment disclosed by the Chen reference fails to describe, either expressly or inherently, an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched *prior to* implanting the refractory metal silicide layer 16 and transforming it back to the amorphous state.

Further, the barrier cap layer 30 disclosed by the Chen reference in the second embodiment thereof is not a dielectric cap *comprising silicon nitride* as recited in independent

claim 24, as proposed to be amended herein, but rather is a polysilicon layer. Thus, independent claim 24, as proposed to be amended herein, is not anticipated by the second embodiment disclosed by the Chen reference.

Independent claim 25, as proposed to be amended herein, recites an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. The operable gate stack comprises a polysilicon layer disposed over the dielectric layer, a non-crystalline metallic silicide film disposed over the polysilicon layer and a dielectric cap comprising silicon nitride on the non-crystalline metallic silicide film.

It is respectfully submitted that the first embodiment of the Chen reference fails to disclose, either expressly or inherently, an operable gate stack comprising, in part, a dielectric cap *comprising silicon nitride* on a non-crystalline metallic silicide film as recited in independent claim 25, as proposed to be amended herein. Rather the dielectric cap of the first embodiment of the Chen reference is an oxide layer (*i.e.,* thin oxide layer 22). Accordingly, it is respectfully submitted that independent claim 25, as proposed to be amended herein, is not anticipated by the first embodiment disclosed by the Chen reference.

Further, the Chen reference fails to disclose, either expressly or inherently, in the second embodiment thereof, an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched *prior to* implanting the refractory metal silicide layer 16 and transforming it back to the amorphous state.

Additionally, the barrier cap layer 30 disclosed by the Chen reference is not a dielectric cap *comprising silicon nitride*, as recited in independent claim 25, as proposed to be amended herein, but rather is a polysilicon layer. As such, it is respectfully submitted that independent claim 25, as proposed to be amended herein, is not anticipated by the second embodiment disclosed by the Chen reference.

Independent claim 26, as proposed to be amended herein, recites a gate stack structure comprising an operable gate stack on a dielectric layer, over a silicon substrate, wherein the

dielectric layer is substantially devoid of pitting. The operable gate stack of claim 26 comprises a metallic silicide film and a dielectric cap comprising silicon nitride on the metallic silicide film.

It is respectfully submitted that the Chen reference, in the first embodiment disclosed therein, fails to describe, either expressly or inherently, a gate stack structure comprising an operable gate stack, the gate stack comprising a dielectric cap *comprising silicon nitride* on a metallic silicide film. Rather, the dielectric cap of the first embodiment of the Chen reference, *i.e.*, the second thin oxide layer 22, is an oxide layer. As such, it is respectfully submitted that independent claim 26, as proposed to be amended herein, is not anticipated by the first embodiment of the Chen reference.

Regarding the second embodiment disclosed by the Chen reference, it is respectfully submitted that a gate stack structure comprising an operable gate stack on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially devoid of pitting is not disclosed, either expressly or inherently. Rather the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched *prior to* implanting the refractory metal silicide layer 16 and transforming it back to the amorphous state.

Additionally, the barrier cap layer 30 disclosed by the second embodiment of the Chen reference is not a dielectric cap *comprising silicon nitride* as recited in independent claim 26, as proposed to be amended herein, but rather is a polysilicon layer. Accordingly, it is respectfully submitted that independent claim 26, as proposed to be amended herein, is not anticipated by the second embodiment disclosed by the Chen reference.

Independent claim 29, as proposed to be amended herein, recites a semiconductor device comprising at least one gate stack which comprises a non-crystalline metallic silicide film and a dielectric cap comprising silicon nitride on the non-crystalline metallic silicide film. The at least one gate stack is formed on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting.

It is respectfully submitted that the Chen reference, in the first embodiment disclosed therein, fails to describe, either expressly or inherently, at least one gate stack comprising, in part, a dielectric cap *comprising silicon nitride* on a non-crystalline metallic silicide film as recited in

independent claim 29, as proposed to be amended herein. Rather, the dielectric cap of the first embodiment disclosed by the Chen reference is an oxide layer, *i.e.*, thin oxide layer 22. Accordingly, it is respectfully submitted that the Chen reference, in the first embodiment thereof, fails to anticipate independent claim 29, as proposed to be amended herein.

Further, a gate stack formed on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting, is not disclosed, either expressly or inherently, in the second embodiment of the Chen reference. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode is etched *prior to* implanting the refractory metal silicide layer 16 and transforming it back to the amorphous state.

Additionally, the cap barrier layer 30 of the second embodiment of the Chen reference is not a dielectric cap *comprising silicon nitride* as recited in independent claim 29, as proposed to be amended herein, but rather is a polysilicon layer. As such, it is respectfully submitted that the Chen reference, in the second embodiment thereof, fails to anticipate independent claim 29, as proposed to be amended herein.

Independent claim 31, as proposed to be amended herein, recites a semiconductor device comprising at least one gate stack structure on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially devoid of pitting, the at least one gate stack structure comprising a metallic silicide film and a dielectric cap comprising silicon nitride on the metallic silicide film.

It is respectfully submitted that the Chen reference, in the first embodiment disclosed therein, fails to describe, either expressly or inherently, at least on gate stack comprising a dielectric cap *comprising silicon nitride* on a metallic silicide film as recited in independent claim 31, as proposed to be amended herein. Rather, the dielectric cap of the first embodiment disclosed by the Chen reference is an oxide layer, *i.e.*, thin oxide layer 22. As such, it is respectfully submitted that the Chen reference, in the first embodiment thereof, fails to anticipate independent claim 31, as proposed to be amended herein.

Further, the Chen reference, in the second embodiment thereof, fails to disclose, either expressly or inherently, a gate stack structure on a dielectric layer wherein the dielectric layer is

substantially devoid of pitting. Rather, the dielectric layer of the structure of the second embodiment of the Chen reference includes pitting as the gate electrode structure is etched *prior to* implanting the refractory metal silicide layer 16 and transforming it back to the amorphous state.

Additionally, the barrier cap layer 30 disclosed by the second embodiment of the Chen reference is not a dielectric cap *comprising silicon nitride* as recited in independent claim 31, as proposed to be amended herein, but rather is a polysilicon layer. Accordingly, it is respectfully submitted that the Chen reference, in the second embodiment thereof, fails to anticipate independent claim 31, as proposed to be amended herein.

In light of the above, it is respectfully submitted that the Chen reference fails to disclose, either expressly or inherently, each and every element of independent claims 23 through 26, 29 and 31, as proposed to be amended herein. As such, these claims are not anticipated by the Chen reference and the withdrawal of the 35 U.S.C. § 102(e) rejection thereof is respectfully requested. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Each of these claims is believed to be in condition for allowance and such favorable action is respectfully requested.

Claims 27 and 28 each depend directly from independent claim 26, claim 30 depends directly from independent claim 29 and claims 32 and 33 each depend directly from independent claim 31. Accordingly, each of these claims is believed to be in condition for allowance for at least the above-cited reasons. As such, withdrawal of the 35 U.S.C. § 102(e) rejection of these claims is respectfully requested as well.

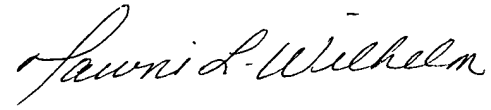
ENTRY OF AMENDMENTS

The proposed amendments to the Title of the Invention and to claims 23 through 26, 29 and 31above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 23 through 33 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Document in ProLaw

Proposed Amendments to the Title:

Applicants propose to amend the Title of the Invention as hereinafter set forth. Please replace the Title of the Invention with the following rewritten Title:

~~--TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE ETCH~~ OPERABLE GATE STACK WHICH IS SUBSTANTIALLY DEVOID OF PITTING AND SEMICONDUCTOR DEVICE COMPRISING SAME--